



# OLED MODULE SPECIFICATION

## ASI-O-223DAYYHE0/M

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (Yellow)	-
3	Duty	1/32	-
4	Resolution	128(H) x 32 (V)	Pixel
5	Active Area	55.02 (W) x 13.10 (H)	mm
6	Panel size	62.00 (W) x 24.00 (H) x 2.00 (D)	mm
7	Module size	62.00 (W) x 60.00 (H) x 2.00 (D)	mm
7	Pixel Pitch	0.43 (W) x 0.41 (H)	mm
8	Pixel Size	0.41 (W) x 0.39 (H)	mm
9	Driver IC	SSD1309	-
10	Interface	8-bit CPU,4-wire SPI,IIC	-
11	Weight	5.82±10%	g



**REVISION RECORD**

<b>REV NO.</b>	<b>REV DATE</b>	<b>CONTENTS</b>	<b>REMARKS</b>
1.0	2013-09-11	First release	
2.0	2014-06-06	Old part # ASI-O-22312832DO-Q-OYS/M	



## **CONTENT**

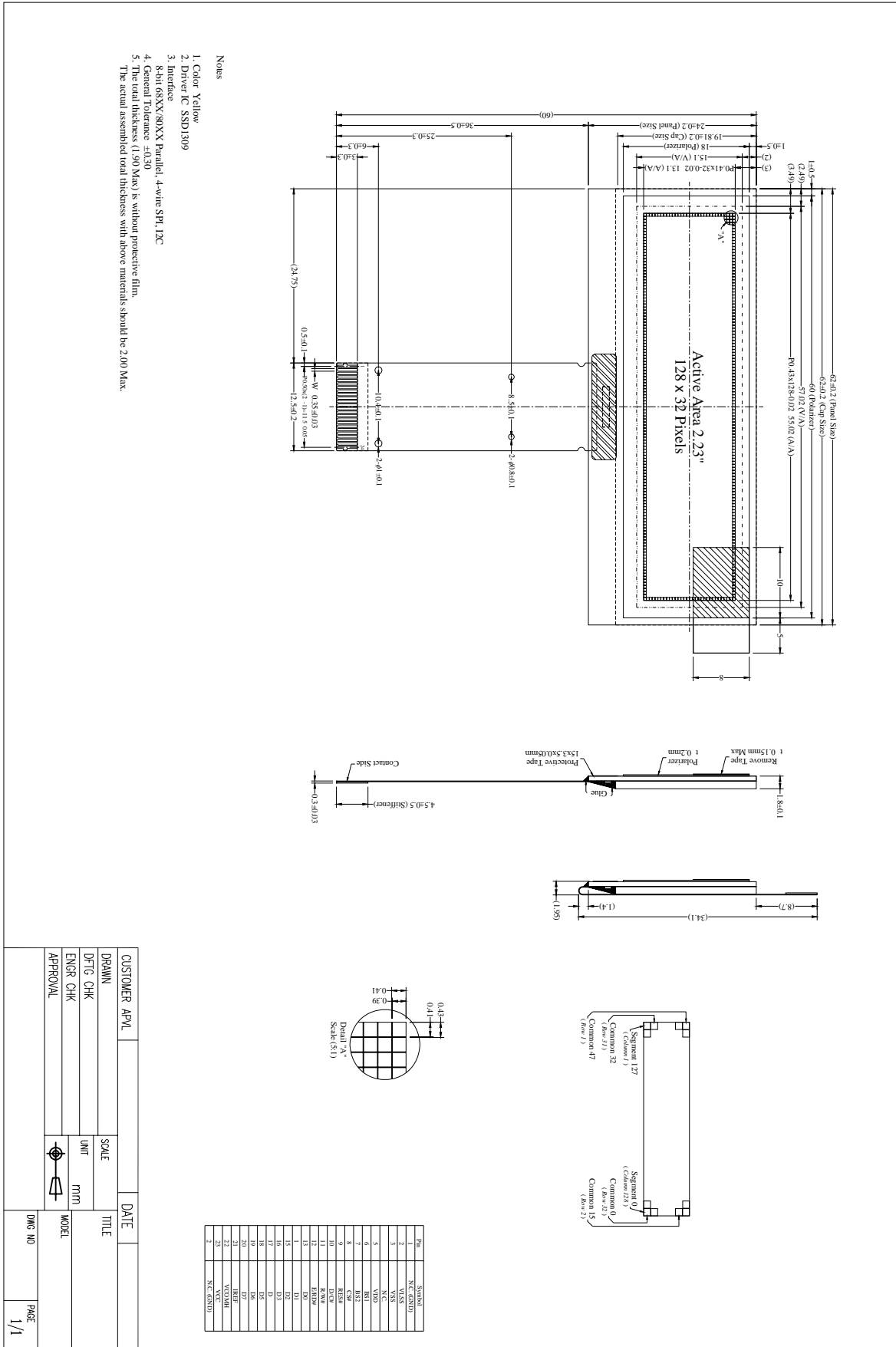
- PHYSICAL DATA
- EXTERNAL DIMENSIONS
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- ELECTRICAL CHARACTERISTICS
- TIMING OF POWER SUPPLY
- ELECTRO-OPTICAL CHARACTERISTICS
- INTERFACE PIN CONNECTIONS
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- OUTGOING QUALITY CONTROL SPECIFICATION
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## ■ PHYSICAL DATA

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## EXTERNAL DIMENSIONS





## ■ ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Min	Typ.	Max	Unit	Notes
Supply voltage for logic	V <sub>DD</sub>	-0.3	-	4	V	1,2
Supply voltage for display	V <sub>CC</sub>	0	-	15.0	V	1,2
Operating temperature	T <sub>OP</sub>	-40	-	85	°C	3
Storage temperature	T <sub>ST</sub>	-40	-	90	°C	3
Life time(120cd/m <sup>2</sup> )	-	40,000	-	-	hour	4
Life time(100cd/m <sup>2</sup> )	-	100,000	-	-	hour	4
Life time(80cd/m <sup>2</sup> )	-	150,000	-	-	hour	4
Humidity	-	-	-	90	%RH	-

Note 1: All the above voltages are on the basis of V<sub>SS</sub> = 0V .

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to electro-optical characteristics . If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V<sub>CC</sub> = 12.5V, T<sub>a</sub> = 25°C, 50% Checkerboard.

Software configuration follows Actual Application Example .

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.



■ ELECTRICAL CHARACTERISTICS

DC Characteristics

Items	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage for logic	$V_{DD}$		1.65	2.8	3.3	V
Supply voltage for display	$V_{CC}$	Note 5	12	12.5	13	V
High level input	$V_{IH}$	$I_{OUT} = 100\mu A, 3.3MH$	$0.8 \times V_{DD}$	-	$V_{DD}$	V
Low level input	$V_{IL}$	$I_{OUT} = 100\mu A, 3.3MH$	0	-	$0.2 \times V_{DD}$	V
High level output	$V_{OH}$	$I_{OUT} = 100\mu A, 3.3MH$	$0.9 \times V_{DD}$	-	$V_{DD}$	V
Low level output	$V_{OL}$	$I_{OUT} = 100\mu A, 3.3MH$	0	-	$0.1 \times V_{DD}$	V
Operating current for $V_{DD}$	$I_{DD}$		-	180	300	$\mu A$
Operating current for $V_{CC}$	$I_{CC}$	Note 6	-	11.4	14.3	mA
		Note 7	-	18.8	23.5	mA
		Note 8	-	36	45	mA
Sleep mode current for $V_{DD}$	$I_{DD,SLEEP}$		-	1	5	$\mu A$
Sleep mode current for $V_{CC}$	$I_{CC,SLEEP}$		-	2	10	$\mu A$

Note 5: Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics and the customer's request.

Note 6:  $V_{DD} = 2.8V, V_{CC} = 12.5V, 30\%$  Display Area Turn on.

Note 7:  $V_{DD} = 2.8V, V_{CC} = 12.5V, 50\%$  Display Area Turn on.

Note 8:  $V_{DD} = 2.8V, V_{CC} = 12.5V, 100\%$  Display Area Turn on.

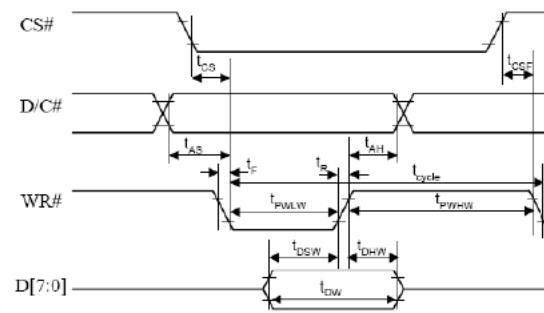
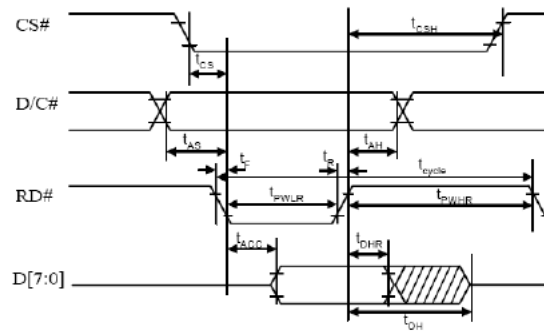
Software configuration follows Actual Application Example .

## ◆ AC Characteristics

### 1. 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	ns
$t_{AS}$	Address Setup Time	20	-	ns
$t_{AH}$	Address Hold Time	0	-	ns
$t_{DW}$	Data Write Time	70	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	ns
$t_{OH}$	Output Disable Time	-	70	ns
$t_{ACC}$	Access Time	-	140	ns
$t_{PWLR}$	Read Low Time	120	-	ns
$t_{PWLW}$	Write Low Time	60	-	ns
$t_{PWHR}$	Read High Time	60	-	ns
$t_{PWHW}$	Write High Time	60	-	ns
$t_{CS}$	Chip Select Setup Time	0	-	ns
$t_{CSH}$	Chip Select Hold Time to Read Signal	0	-	ns
$t_{CSF}$	Chip Select Hold Time	20	-	ns
$t_R$	Rise Time	-	40	ns
$t_F$	Fall Time	-	40	ns

\* ( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )



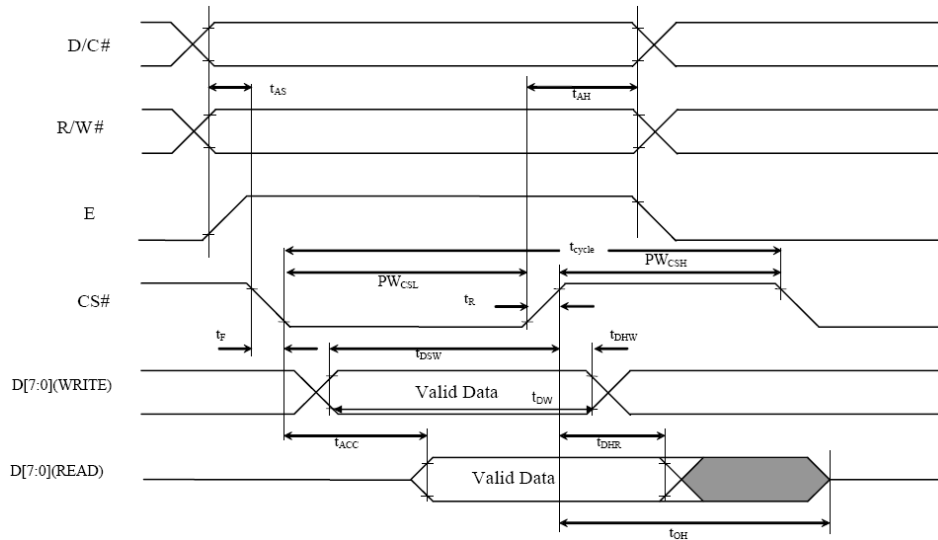




## 2. 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	ns
$t_{AS}$	Address Setup Time	20	-	ns
$t_{AH}$	Address Hold Time	0	-	ns
$t_{DW}$	Data Write Time	80	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	ns
$t_{DHW}$	Write Data Hold Time	20	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	ns
$t_{OH}$	Output Disable Time	-	70	ns
$t_{ACC}$	Access Time	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
$PW_{CSH}$	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
$t_R$	Rise Time	-	40	ns
$t_F$	Fall Time	-	40	ns

\* ( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )



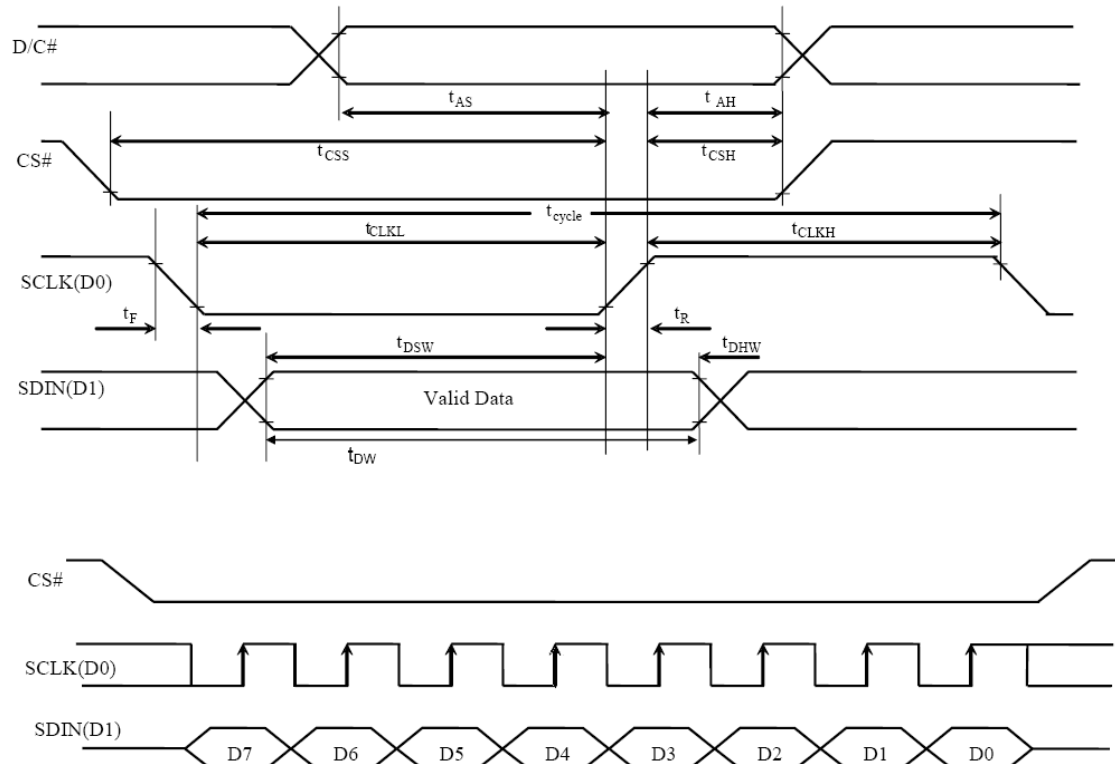


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## 3. Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	ns
$t_{AS}$	Address Setup Time	15	-	ns
$t_{AH}$	Address Hold Time	15	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	ns
$t_{CSH}$	Chip Select Hold Time	50	-	ns
$t_{DW}$	Data Write Time	55	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	ns
$t_{CLKL}$	Clock Low Time	50	-	ns
$t_{CLKH}$	Clock High Time	50	-	ns
$t_R$	Rise Time	-	40	ns
$t_F$	Fall Time	-	40	ns

\* ( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )

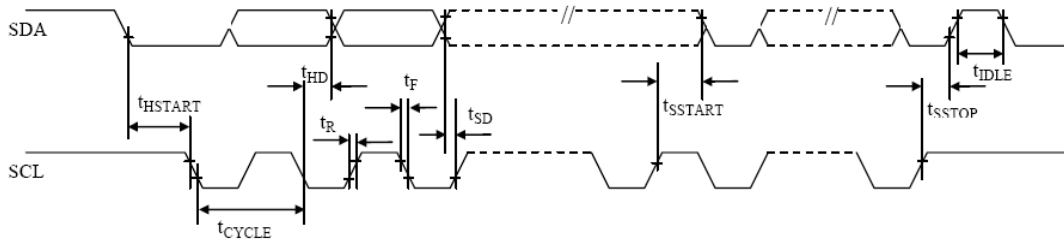




## 4. I<sup>2</sup>C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	2.5	-	$\mu\text{s}$
$t_{\text{HSTART}}$	Start Condition Hold Time	0.6	-	$\mu\text{s}$
$t_{\text{HD}}$	Data Hold Time (for "SDA <sub>OUT</sub> " Pin)	0	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " Pin)	300		
$t_{\text{SD}}$	Data Setup Time	100	-	ns
$t_{\text{SSTART}}$	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	$\mu\text{s}$
$t_{\text{SSTOP}}$	Stop Condition Setup Time	0.6	-	$\mu\text{s}$
$t_{\text{R}}$	Rise Time for Data and Clock Pin		300	ns
$t_{\text{F}}$	Fall Time for Data and Clock Pin		300	ns
$t_{\text{IDLE}}$	Idle Time before a New Transmission can Start	1.3	-	$\mu\text{s}$

\* ( $V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ )



## ■ TIMING OF POWER SUPPLY

### 1. Commands

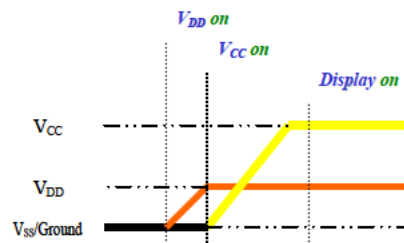
Refer to the Technical Manual for the SSD1309

### 2. Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

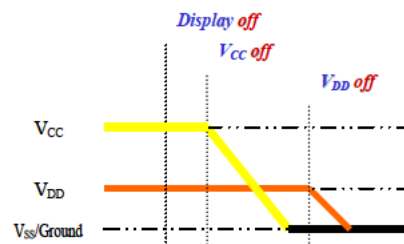
#### 2.1 Power up Sequence:

1. Power up  $V_{DD}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



#### 2.2 Power down Sequence:

1. Send Display off command
2. Power down  $V_{CC}$
3. Delay 100ms  
(When  $V_{CC}$  is reach 0 and panel is completely discharges)
4. Power down  $V_{DD}$



#### Note 9:

- 1) Since an ESD protection circuit is connected between  $V_{DD}$  and  $V_{CC}$  inside the driver IC,  $V_{CC}$  becomes lower than  $V_{DD}$  whenever  $V_{DD}$  is ON and  $V_{CC}$  is OFF.
- 2)  $V_{CC}$  should be kept float (disable) when it is OFF.
- 3) Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- 4)  $V_{DD}$  should not be power down before  $V_{CC}$  power down.

### 3. Reset Circuit

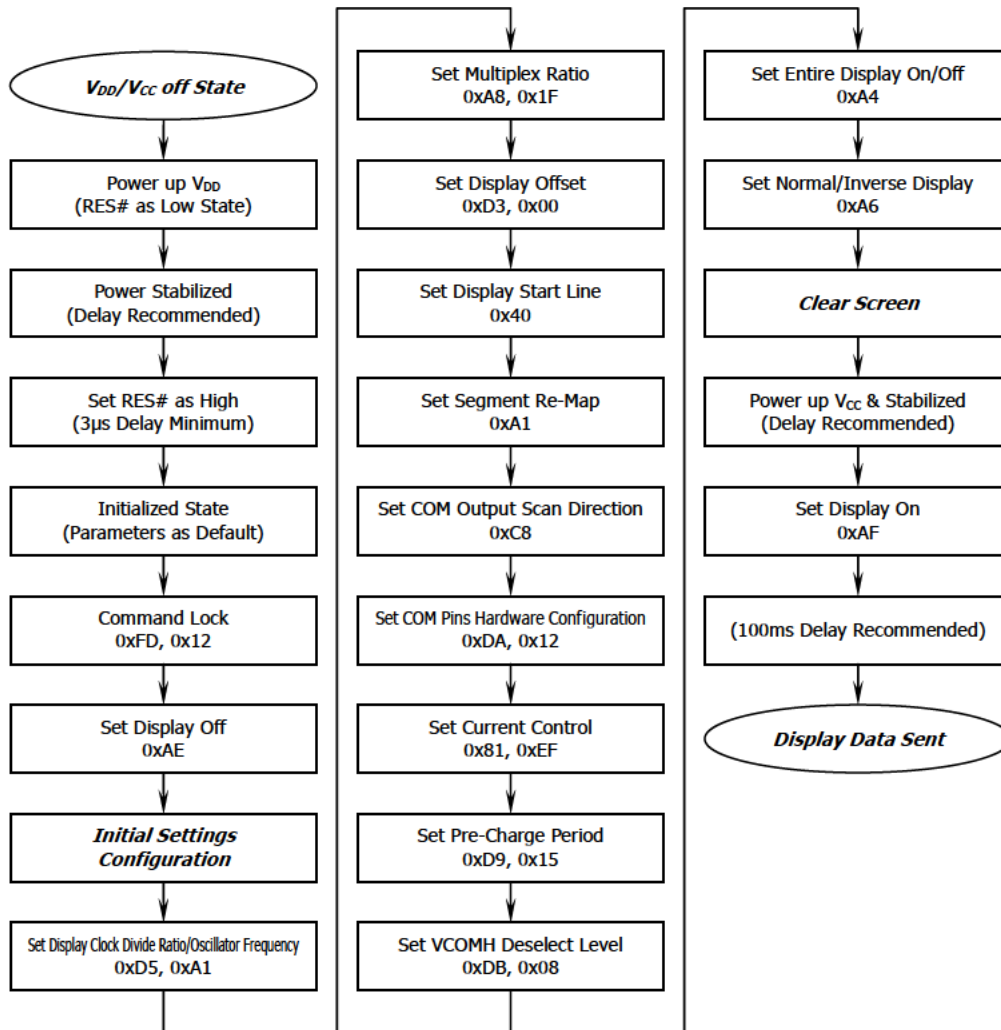
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×32 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

## 4. Actual Application Example

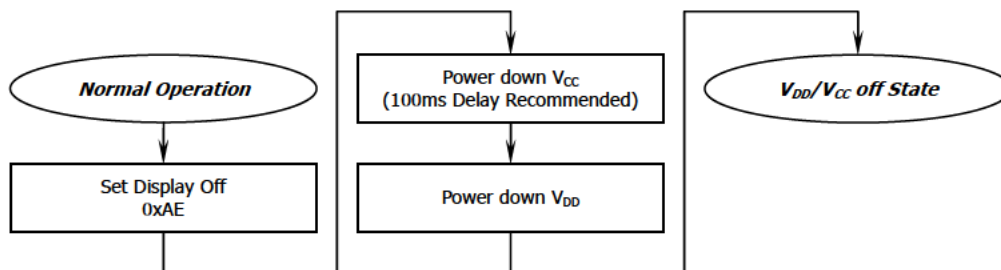
Command usage and explanation of an actual example

<Power up Sequence>

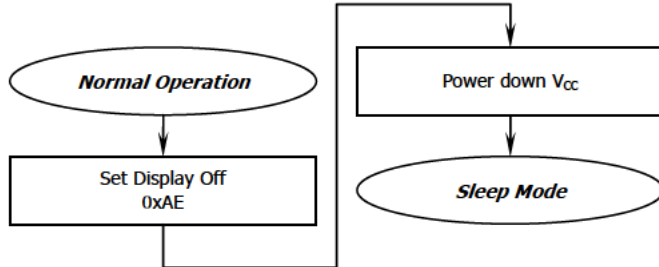


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

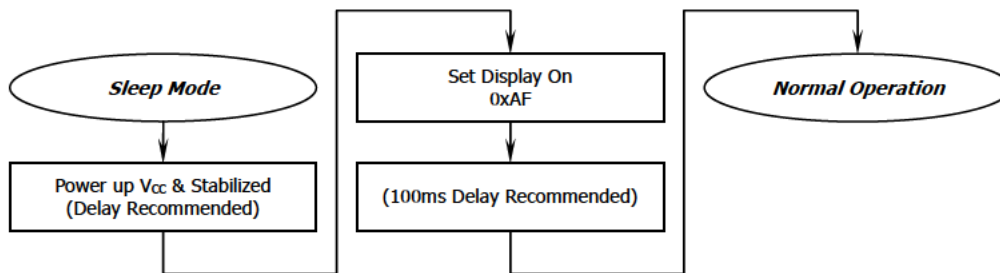
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items	Symbol	Min.	Typ.	Max.	Unit	Remark	
Operating Luminance	L	100	120	-	cd /m <sup>2</sup>	Yellow	
Color Coordinate	Yellow	CIE x	0.46	0.50	0.54	CIE1931	Darkroom
		CIE y	0.45	0.49	0.53		
Contrast Ratio	Cr	-	>10,000:1	-		Darkroom	
Viewing Angle Uniformity	△ θ	-	Free	-	Degree	-	

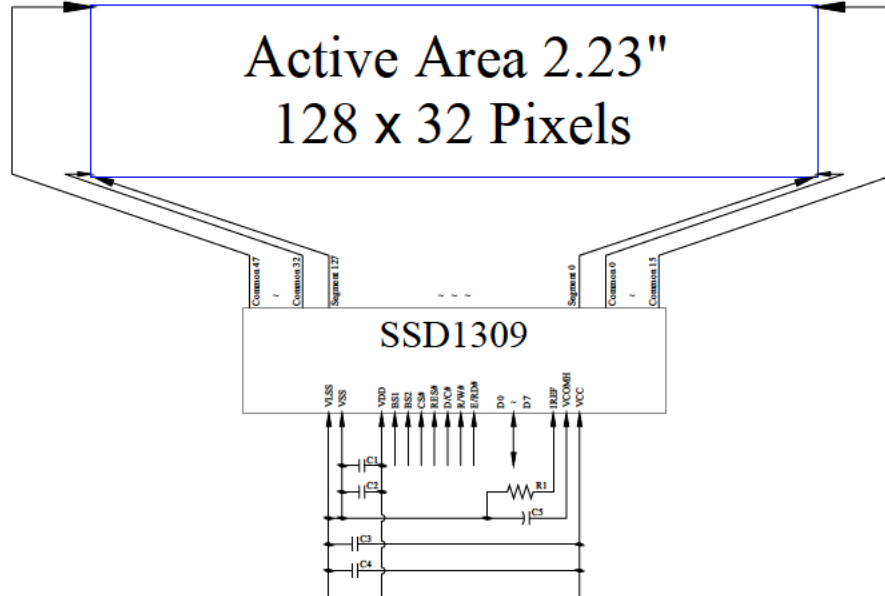
Note : Brightness (L<sub>br</sub>) is subject to the change of the panel characteristics and the customer's request.

Optical measurement taken at V<sub>DD</sub> = 2.8V, V<sub>CC</sub> = 12.5V.

Software configuration follows Actual Application Example .

## ■ INTERFACE PIN CONNECTIONS

### 1. Block Diagram



MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1 $\mu$ F

C2: 4.7 $\mu$ F

C4: 10 $\mu$ F

C5: 4.7 $\mu$ F / 25V Tantalum Capacitor

R1: 910k $\Omega$ , R1 = (Voltage at IREF - BGGND) / IREF



## 2. Pin Definition

Pin Number	Symbol	I/O	Function															
<b>Power Supply</b>																		
5	VDD	P	<b>Power Supply for Logic Circuit</b> This is a voltage supply pin. It must be connected to external source.															
3	VSS	P	<b>Ground of Logic Circuit</b> This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.															
23	VCC	P	<b>Power Supply for OEL Panel</b> This is the most positive voltage supply pin of the chip. It must be supplied externally.															
2	VLSS	P	<b>Ground of Analog Circuit</b> This is an analog ground pin. It should be connected to V <sub>SS</sub> externally.															
<b>Driver</b>																		
21	IREF	I	<b>Current Reference for Brightness Adjustment</b> This pin is segment current reference pin. A resistor should be connected between this pin and V <sub>SS</sub> . Set the current at 10μA.															
22	VCOMH	O	<b>Voltage Output High Level for COM Signal</b> This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V <sub>SS</sub> .															
<b>Interface</b>																		
6 7	BS1 BS2	I	<b>Communicating Protocol Select</b> These pins are MCU interface selection input. See the following table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>I<sup>2</sup>C</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire Serial</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>0</td> <td>1</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		BS1	BS2	I <sup>2</sup> C	1	0	4-wire Serial	0	0	8-bit 68XX Parallel	0	1	8-bit 80XX Parallel	1	1
	BS1	BS2																
I <sup>2</sup> C	1	0																
4-wire Serial	0	0																
8-bit 68XX Parallel	0	1																
8-bit 80XX Parallel	1	1																
9	RES#	I	<b>Power Reset for Controller and Driver</b> This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.															
8	CS#	I	<b>Chip Select</b> This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.															
10	D/C#	I	<b>Data/Command Control</b> This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I <sup>2</sup> C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
12	E/RD#	I	<b>Read/Write Enable or Read</b> This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I <sup>2</sup> C mode is selected, this pin must be connected to V <sub>SS</sub> .															
11	R/W#	I	<b>Read/Write Select or Write</b> This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I <sup>2</sup> C mode is selected, this pin must be connected to V <sub>SS</sub> .															





# ASI-O-223DAYYHE0/M

Pin Number	Symbol	I/O	Function
<b>Interface (Continued)</b>			
13~20	D0~D7	I/O	<b>Host Data Input/Output Bus</b> These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDA <sub>OUT</sub> , SDA <sub>IN</sub> in application and D0 is the serial clock input, SCL. Unused pins must be connected to V <sub>SS</sub> except for D2 in serial mode.
<b>Reserve</b>			
4	N.C.	-	<b>Reserved Pin</b> The N.C. pin between function pins is reserved for compatible and flexible design.
1, 24	N.C. (GND)	-	<b>Reserved Pin (Supporting Pin)</b> The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.



■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		90±2°C, 500 hours	<ol style="list-style-type: none"> <li>1. After testing, the function test is ok.</li> <li>2. After testing, no addition to the defect.</li> <li>3. After testing, the change of luminance should be within +/- 50% of initial value.</li> <li>4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.</li> <li>5. After testing, the change of total current consumption should be within +/- 50% of initial value.</li> </ol>
High Temperature Operating (HTO)		85±2°C, 500 hours	
Low Temperature Storage (LTS)		-40±2°C, 500 hours	
Low Temperature Operating (LTO)		-40±2°C, 500 hours	
High Temperature / High Humidity Storage (HTHHS)		60±3°C, 90%±3%RH, 240 hours	
Thermal Shock (Non-operation) (TS)		-40±2°C ~ 25°C ~ 85±2°C (30min) (5min) (30min) 100cycles	
Vibration (Packing)	10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z	<ol style="list-style-type: none"> <li>1. One box for each test.</li> <li>2. No addition to the cosmetic and the electrical defects.</li> </ol>	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.  
 2) The HTHHS test is requested the Pure Water(Resistance > 10MΩ).

## ■ OUTGOING QUALITY CONTROL SPECIFICATION

### ◆ Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

### ◆ Sampling Plan

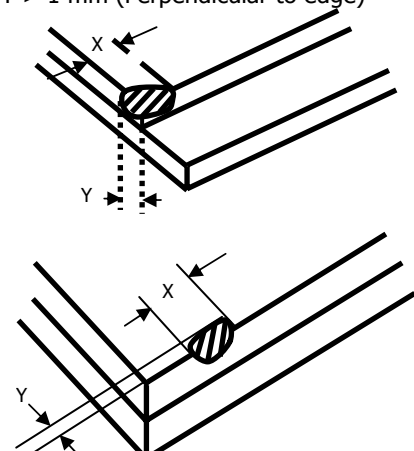
Level II, Normal Inspection, Single Sampling, MIL-STD-105E

### ◆ Criteria and Acceptable Quality Level

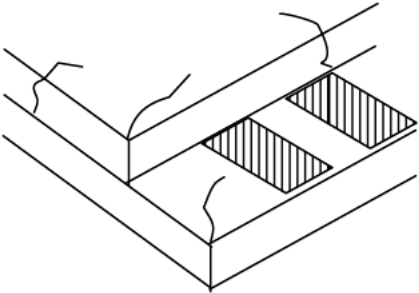


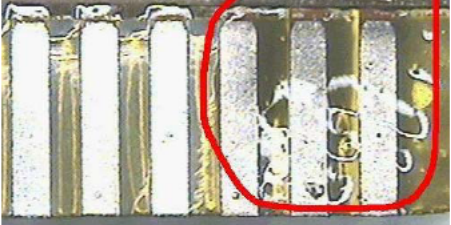
Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

### ◆ Inspection Criteria

#### 1.1 Cosmetic Check (Display Off) in Non-Active Area

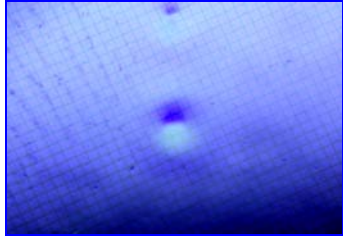
Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>X &gt; 6 mm (Along with Edge) Y &gt; 1 mm (Perpendicular to edge)</p> 

1.2 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	<p>Any crack is not allowable.</p> 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

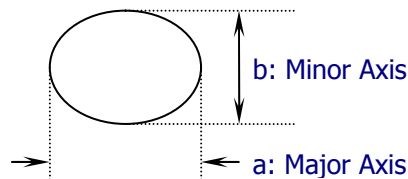
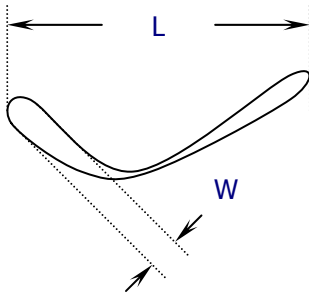
## 1.3 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

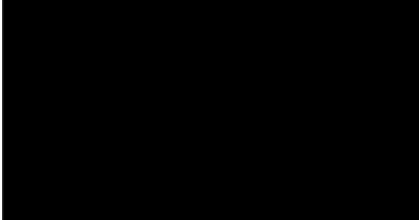
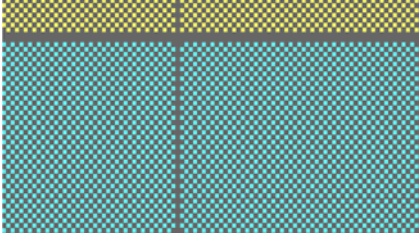
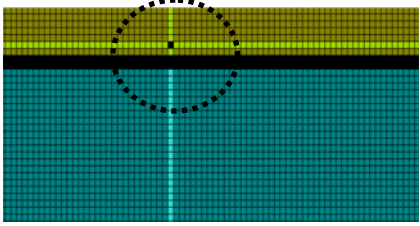
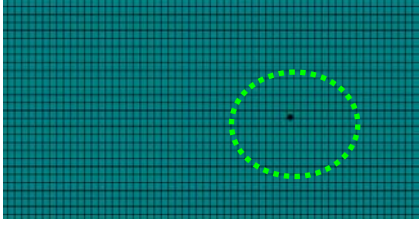
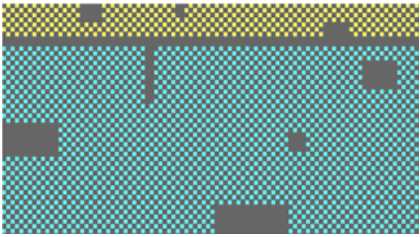
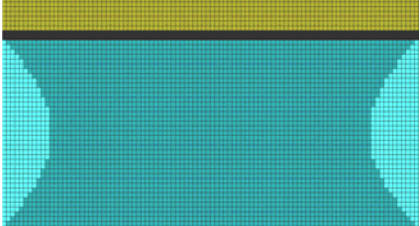
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

\* Protective film should not be tear off when cosmetic check.

\*\* Definition of W & L &  $\Phi$  (Unit: mm):  $\Phi = (a + b) / 2$



## 1.4 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	



## ■ CAUTIONS IN USING OLED MODULE

### ◆ Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
  - i. Avoid drop from high, avoid excessive impact and pressure.
  - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
  - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
  - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
  - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
  - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
  - i. Be sure to ground the body when handling the OLED Modules.
  - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
  - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
  - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
  - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
  - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence:  $V_{DD} \rightarrow V_{PP}$ , and power off sequence:  $V_{PP} \rightarrow V_{DD}$ .
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.



13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

## ◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature :  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

## ◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between  $0^{\circ}\text{C}$  and  $30^{\circ}\text{C}$  , the relative humidity not over 60%.

## ◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

## ◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.