ALL SHORE INDUSTRIES

ASI-O-240FAWWH60/M

Item	Specification	Unit
Display Mode	Passive Matrix OLED	/
Display Color	Monochrome (White)	/
Duty	1/64	/
Resolution (H × V)	128 × 64	Pixel
Active Area (W × H)	55.01 × 27.49	mm^2
Panel Size (W × H × D)	60.50 × 37.00 × 1.80	mm^3
Module Size (W × H × D)	60.50 × 73.00 × 1.80	mm^3
Pixel Pitch (W × H)	0.43 × 0.43	mm^2
Pixel Size (W × H)	0.40 × 0.40	/
Driver IC	SSD1309	
Interface Type	8-bit 68XX/80XX parallel, 4-wire SPI, IIC	/
Weight	TBD	g

■ REVISION RECORD

REV NO.	REV DATE	CONTENTS	REVISED PAGE NO.
1.0	2022-10-25	First Release	

CONTENTS

■ PHYSICAL DATA

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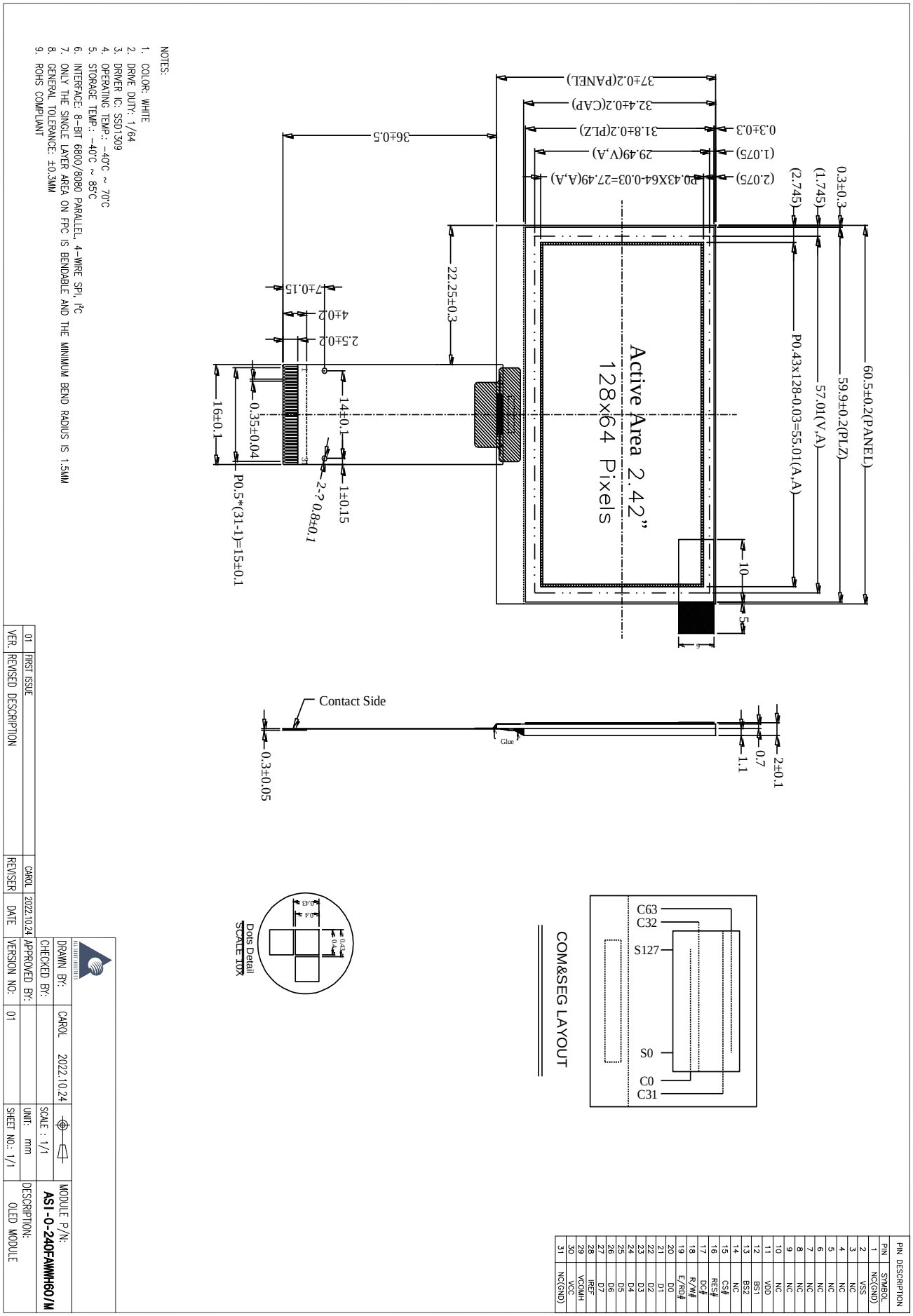
Pixel Size (W × H)	0.40 × 0.40	/
Driver IC	SSD1309	/
Interface Type	8-bit 68XX/80XX parallel, 4-wire SPI, IIC	/
Weight	TBD	g

Note 1: ROHS compliant;
Note 2: OLED weight tolerance: ±5%.

■ EXTERNAL DIMENSIONS



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4.0	V	1,2
Supply Voltage for Display	V_{CC}	8	17.0	V	1,2
Operating Temperature	T_{OP}	-40	70	℃	-
Storage Temperature	T_{ST}	-40	85	℃	3
Life Time (220cd/m²)	-	13,000	-	Hour	4
Life Time (200cd/m²)	-	15,000	-	Hour	4
Life Time (180cd/m²)	-	16,000	-	Hour	4

Note 1: All the above voltages are on the basis of "V_{SS}=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to "Electro-Optical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

Note 4: (1) Setting of 220 cd/m^2:
- Contrast setting: 0x44
- Frame rate: 105Hz
- Duty setting: 1/64

(2) Setting of 200 cd/m^2:
- Contrast setting: 0x3e
- Frame rate: 105Hz
- Duty setting: 1/64

(3) Setting of 180 cd/m^2:
- Contrast setting: 0x37
- Frame rate: 105Hz
- Duty setting: 1/64

■ ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

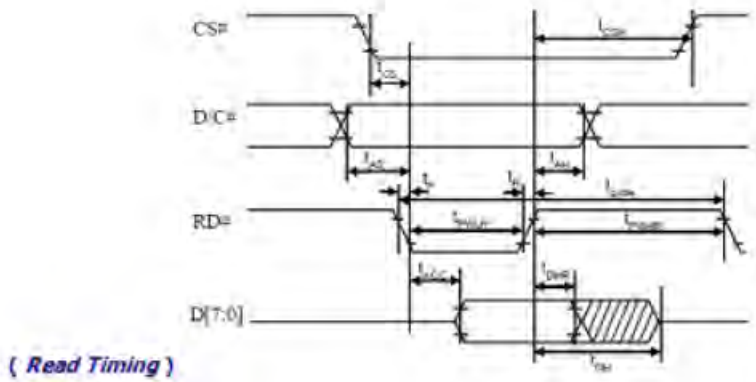
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage for Logic	V_{DD}	-	1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}		12	12.5	13	V
High Level Input	V_{IH}		0.8V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.2V_{DD}	V
High Level Output	V_{OH}	I_{OUT}=100μA,3.3 MHz	0.9V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT}=100μA,3.3 MHz	0	-	0.1V_{DD}	V
VDD Supply Current VDD=2.8V, VCC=12, IREF=10uA, no panel attached, Display ON, All ON	I_{DD}	Contrast=FFh	-	90	110	μA
VCC Supply Current VDD=2.8V, VCC=12, IREF=10uA, no panel attached, Display ON, All ON	I_{CC}		-	450	580	μA
Segment Output Current, VDD=2.8V, VCC=12, REF=10uA, Display ON.	I_{SEG}	Contrast=FFh	280	310	340	μA
		Contrast=AFh	-	215	-	
		Contrast=7Fh	-	155	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	20	-	-	
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$	VDD=1.65V~3.3V, VCC=7V~16V, Display OFF, No panel attached	-	-	10	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$	VDD=1.65V~3.3V, VCC=7V~16V, Display OFF, No panel attached	-	-	10	μA

◆ AC Characteristics

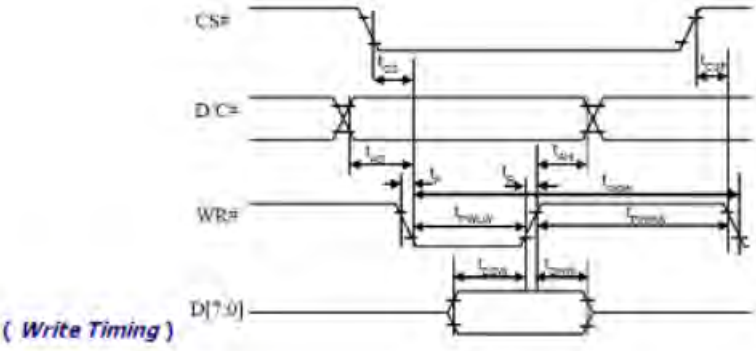
1. 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min.	Max.	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS}=1.65V to 3.3V, Ta=25℃)



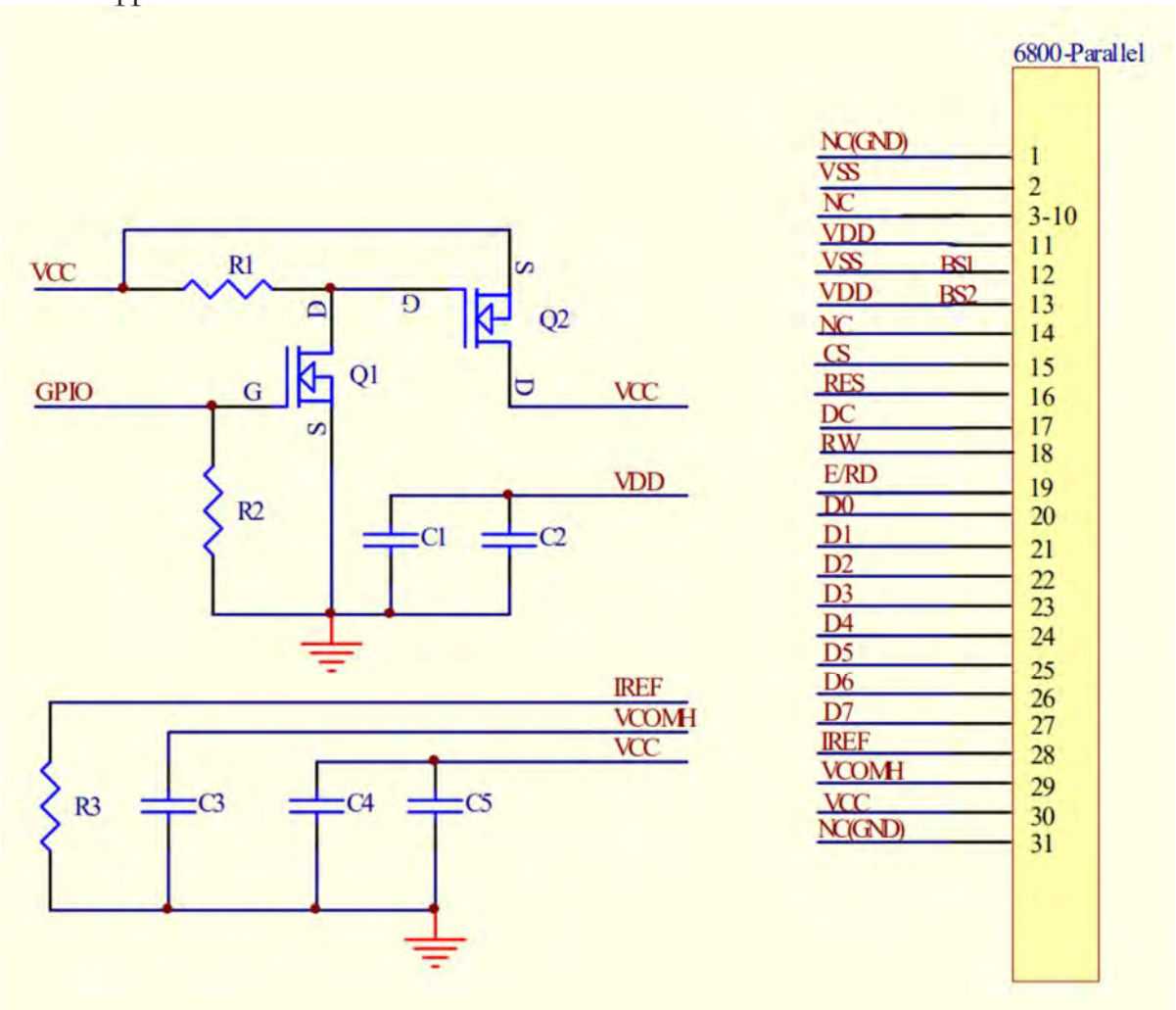
(Read Timing)



(Write Timing)

1.1 68XX-Series MPU Parallel Interface

Please designing the electronic switch circuit on user's main board, otherwise current leakage could happen.



Recommended Components:

C1,C2: 1μF / 16V, X5R
C3: 2.2μF / 25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF / 25V, X7R
R1,R2: 47 kΩ
R3: 910kΩ, R3=(Voltage at IREF-VSS)/IREF
Q1: FDN338P
Q2: FDN335N

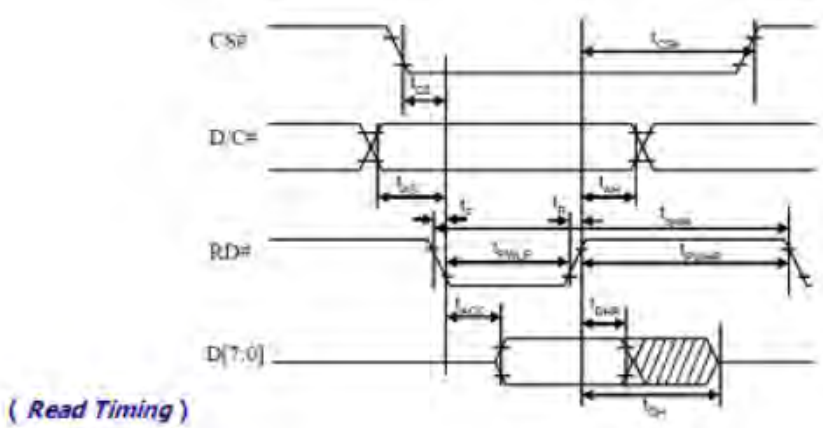
Note:

VDD: 1.65~3.3V
VCC_IN: 11.5V~12.5V

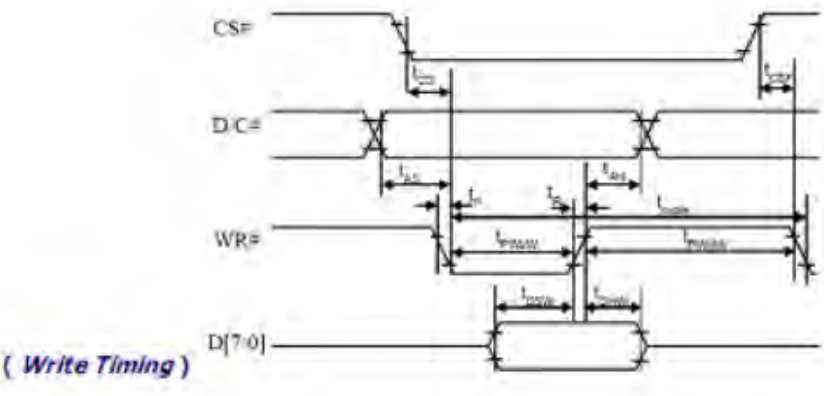
2. 80XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min.	Max.	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS}=1.65V to 3.3V, Ta=25℃)



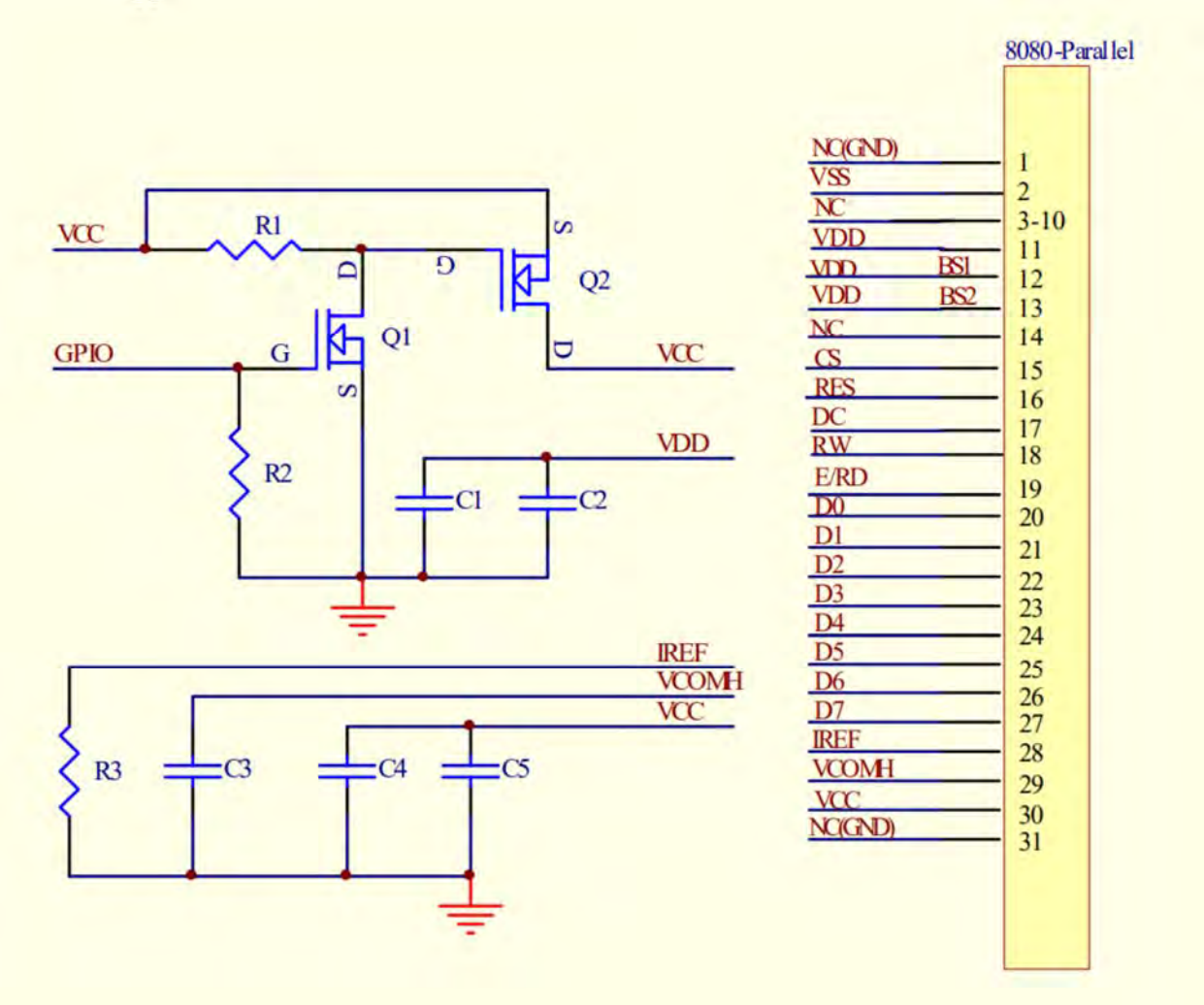
(Read Timing)



(Write Timing)

2.1 80XX-Series MPU Parallel Interface

Please designing the electronic switch circuit on user's main board, otherwise current leakage could happen.



Recommended Components:

C1,C2: 1µF / 16V, X5R
C3: 2.2µF / 25V
C4: 4.7µF / 25V, X7R
C5: 0.1µF / 25V, X7R
R1,R2: 47 kΩ
R3: 910kΩ, R3=(Voltage at IREF-VSS)/IREF
Q1: FDN338P
Q2: FDN335N

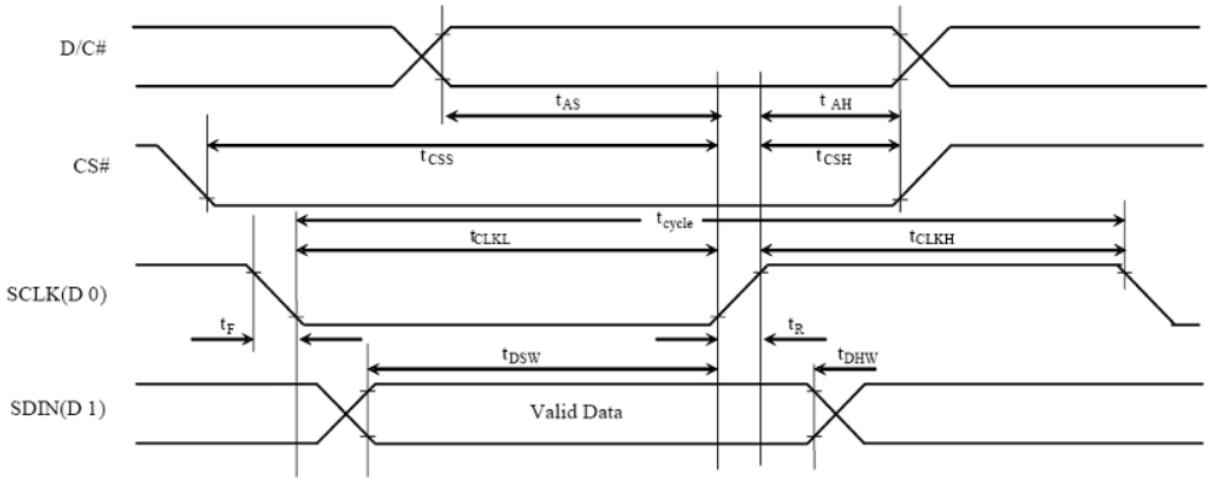
Note:

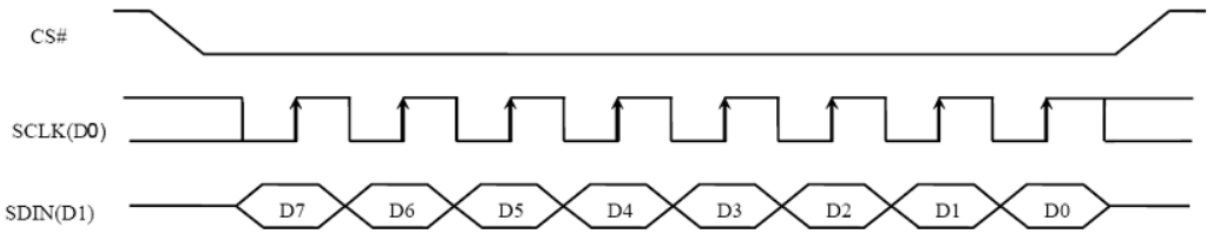
VDD: 1.65~3.3V
VCC_IN: 11.5V~12.5V

3. Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

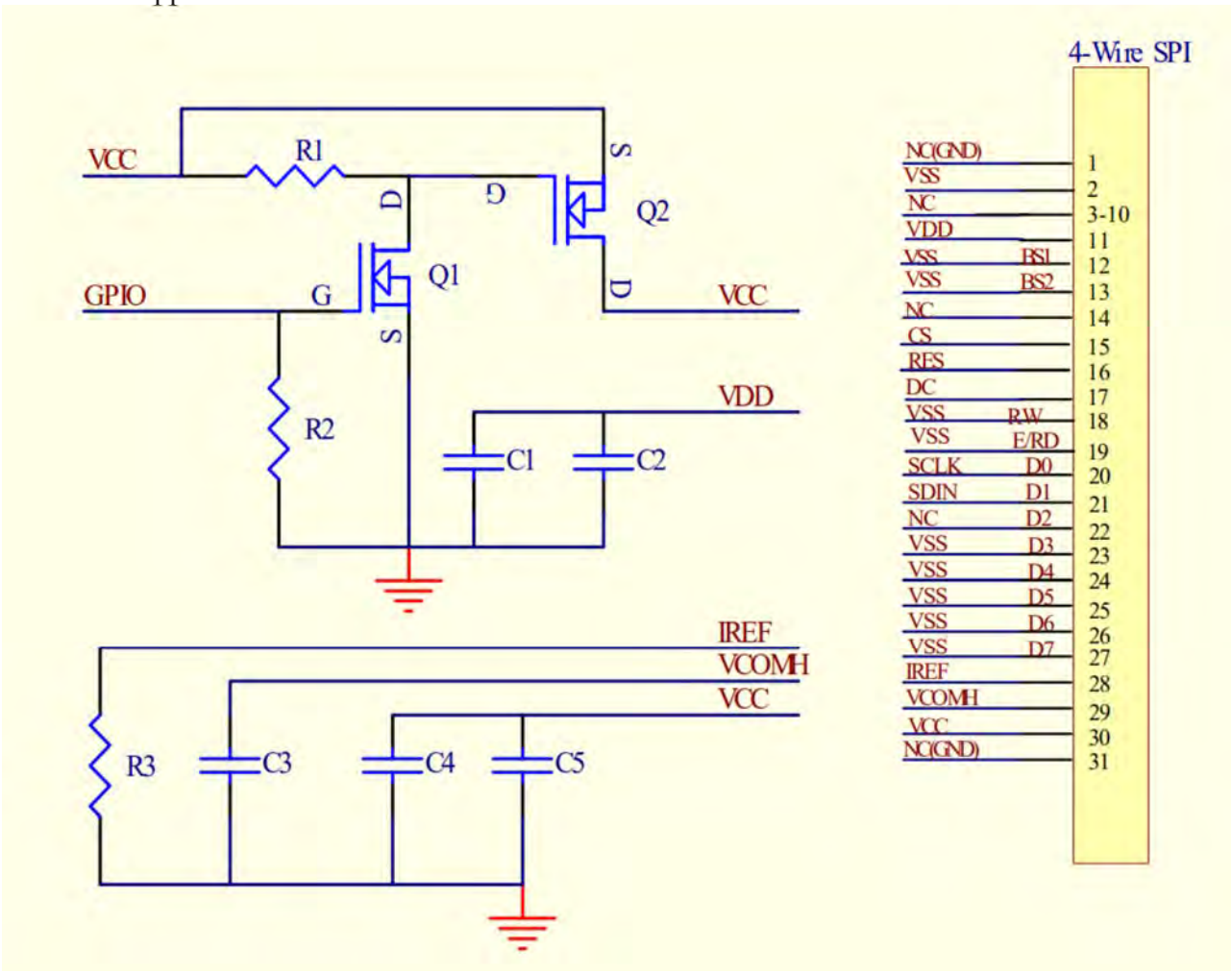
* (V_{DD} - V_{SS}=1.65V to 3.3V, Ta=25℃)





3.1 4-wire Series Interface

Please designing the electronic switch circuit on user's main board, otherwise current leakage could happen.



Recommended Components:

C1,C2: 1μF / 16V, X5R
C3: 2.2μF / 25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF / 25V, X7R
R1,R2: 47 kΩ
R3: 910kΩ, R3=(Voltage at IREF-VSS)/IREF
Q1: FDN338P
Q2: FDN335N

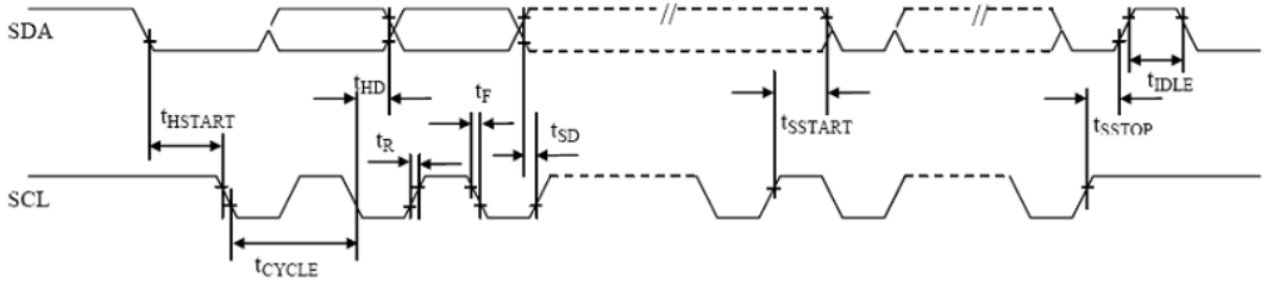
Note:

VDD: 1.65~3.3V
VCC_IN: 11.5V~12.5V

4. I²C Interface Timing Characteristics

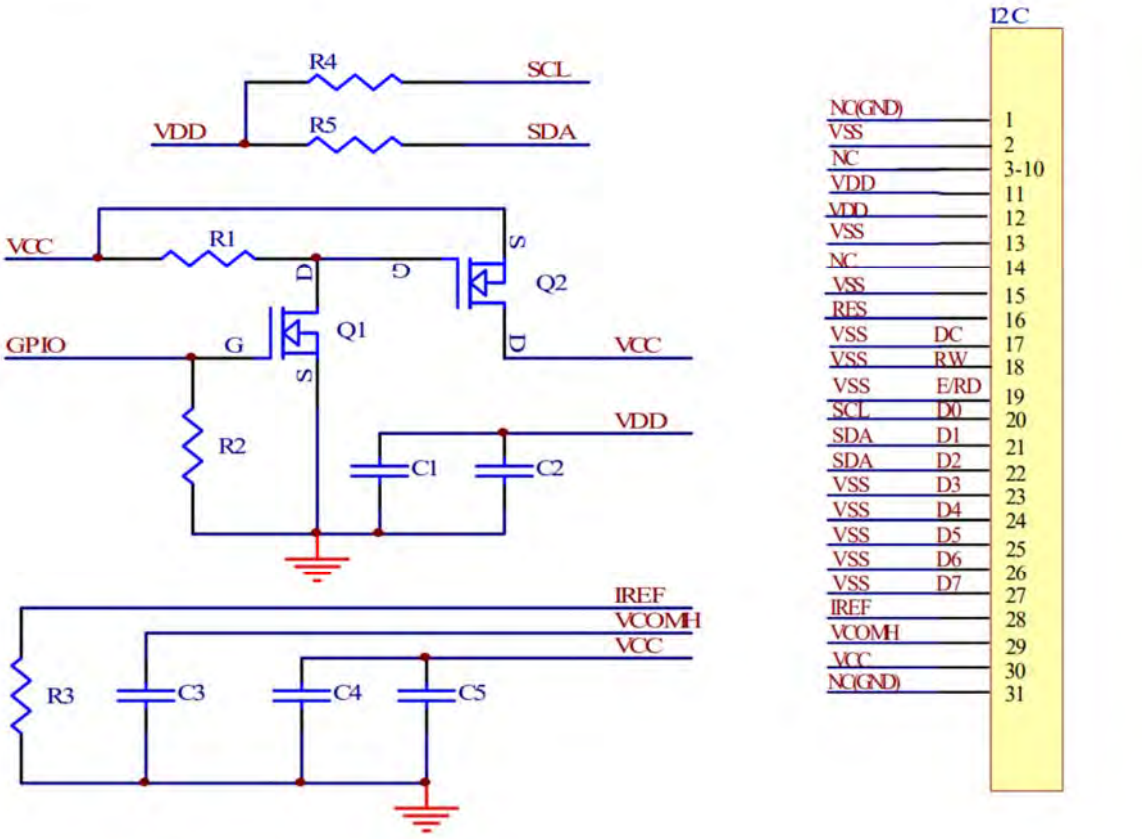
Symbol	Description	Min.	Max.	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DD} - V_{SS}=1.65V to 3.3V, Ta=25℃)



4.1 I^2CInterface with Internal Charge Pump

Please designing the electronic switch circuit on user's main board, otherwise current leakage could happen.



Recommended Components:

C1,C2: 1μF / 16V, X5R
C3: 2.2μF / 25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF / 25V, X7R
R1,R2: 47 kΩ
R3: 910kΩ, R3=(Voltage at IREF-VSS)/IREF
R4, R5: 4.7 kΩ
Q1: FDN338P
Q2: FDN335N
Note:
VDD: 1.65~3.3V
VCC_IN: 11.5V~12.5V

The I^2C slave address is 0111100b'. If the customer ties D/C# to VDD, the I^2C slave address will be 0111101b'.

■ TIMING OF POWER SUPPLY

1. Commands

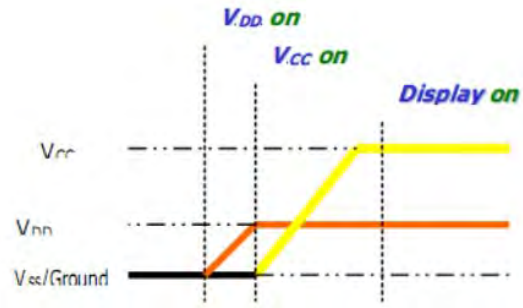
Refer to the Technical Manual for the SSD1309.

2. Power Down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up / down routine should include a delay period between high voltage and low voltage power sources during turn on / off. It gives the OEL panel enough time to complete the action of charge and discharge before / after the operation.

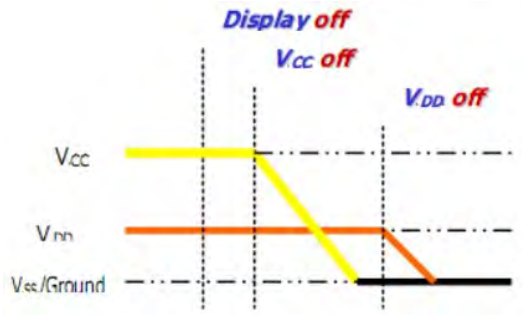
2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 8:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

3. Reset Circuit Power

When RES# input is low, the chip is initialized with the following status:

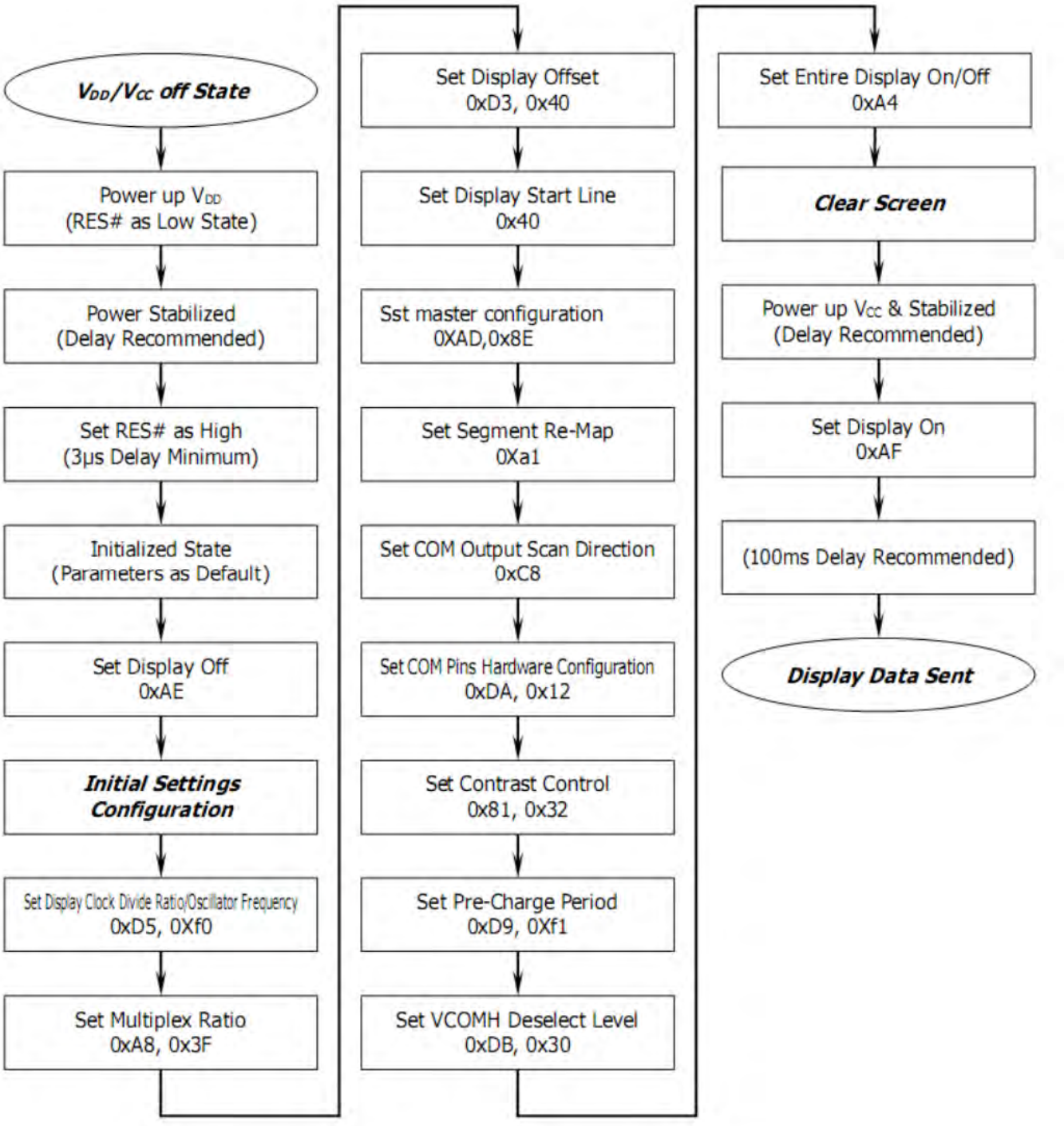
1. Display is OFF
2. 128 × 64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4. Actual Application Example

Command usage and explanation of an actual example

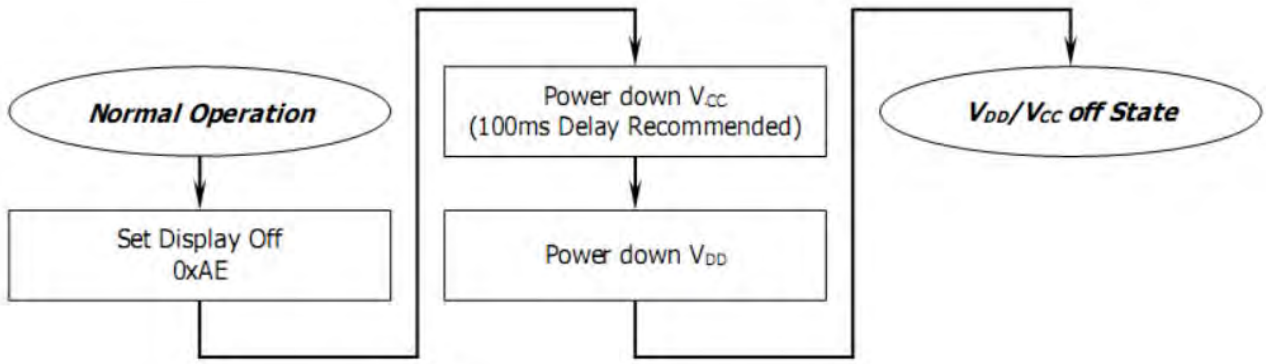
4.1 V_{CC} Supplied Externally

<Power up Sequence>

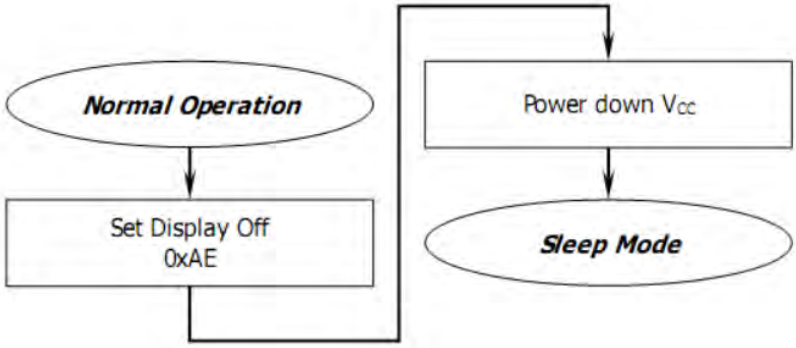


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

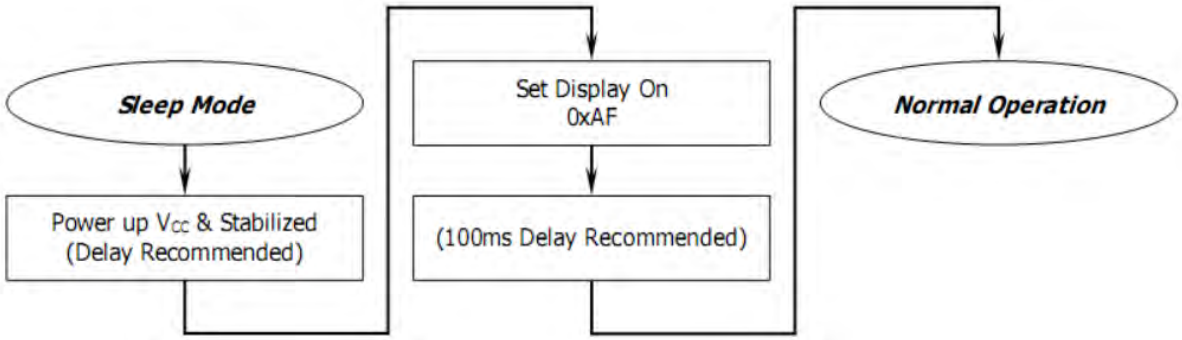
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```
void SSD1309()
{
      RES=0;
      delay(1000);
      RES=1;
      delay(1000);

         write_i(0xae); /*set display off*/

         write_i(0x00); /*set lower column address*/
         write_i(0x10); /*set higher column address*/

         write_i(0x40); /*set display start line*/

         write_i(0x81); /*set contract control*/
```

```
        write_i(0x32);

        write_i(0xa1); /*set segment remap*/

        write_i(0xa6); /*set normal display*/

        write_i(0xa8); /*set multiplex ratio*/
        write_i(0x3f); / 1/64*/

        write_i(0xc8); /*set com scan direction*/

        write_i(0xD3); /*set display offset*/
        write_i(0x00);

        write_i(0xD5); /*set display clock divide/oscillator frequency*/
        write_i(0xa0);

        write_i(0xd9);
        write_i(0xf1);

        write_i(0xda); /*set com pin configuartion*/
        write_i(0x12);

        write_i(0x91);
        write_i(0x3f);
         write_i(0x3f);
          write_i(0x3f);
           write_i(0x3f);

        write_i(0xaf); /*set display on*/
}

void write_i(unsigned char ins)
{
      RS=0;
      CS=0;
      WR=0;
      P1=ins;
      WR=1;
      CS=1;
}

void write_d(unsigned char dat)
{
      RS=1;
      CS=0;
      WR=0;
      P1=dat;
      WR=1;
      CS=1;
}

void delay(unsigned int t)
{
while(i>0)
{
i--;
}
}
```

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Normal Mode Current Consumption		-	-	43	52	mA	All pixels on
Standby Mode Current Consumption		-	-	0.5	1.5	mA	Standby mode 10% pixels on
Normal Mode Power Consumption		-	-	TBD	TBD	mW	All pixels on
Standby Mode Power Consumption		-	-	6.5	19.5	mW	Standby mode 10% pixels on
Brightness		Lbr	90	110	-	cd/m^2	White
Color Coordinate	White	CIE x	0.24	0.28	0.32	CIE1931	Darkroom
		CIE y	0.28	0.32	0.36		
Contrast Ratio		Cr	2000:1	-	-	-	Darkroom
Viewing Angle Uniformity		Δθ	160	-	-	Degree	-

Note:
VDD is 2.8V, set VDD selection (0xad)=(0x40),
VDD is 1.8V, set VDD selection (0xad)=(0x60) contrast setting is shown below.

(1) Normal mode condition:
- Driving voltage: 12V
- Contrast setting: 0x3e
- Frame rate: 105Hz
- Duty setting: 1/64

(2) Standby mode condition:
- Driving voltage: 12V
- Contrast setting: 0x00
- Frame rate: 105Hz
- Duty setting: 1/64

■ INTERFACE DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>11</td><td>VDD</td><td>P</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>2</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>30</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>28</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and Vss. Set the current at 12.5μA maximum.</td></tr>
<tr><td>29</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and Vss.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>16</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>12
13</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS1</td><td>BS2</td></tr>
<tr><td>I^2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>15</td><td>CS#</td><td>I</td><td>Chip Select
This pin is chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>17</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the timing characteristics Diagrams.</td></tr>
<tr><td>19</td><td>E/RD#</td><td>I</td><td>Read / Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable(E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

18	R/W#	I	**Read / Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I^2C mode is selected, this pin must be connected to V_{SS}.
20~27	D0~D7	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL. Unused pins must be connected to Vss except for D2 in serial mode.
Reserve			
1 3~10 14 31	N.C.(GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

■ RELIABILITY TEST

No.	Test Item		Test Condition	Remark
1	High Temperature Storage Test		85℃ ± 2℃ / 120Hrs.	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within ±50% of initial value. 4. After testing, the change for the mono and area color must be within (±0.02, ±0.02) and for the full color it must be within (±0.04, ±0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within ±50% of initial value.
2	Low Temperature Storage Test		-40℃± 2℃ / 120Hrs.	
3	High Temperature Operating Test		70℃ ± 2℃ / 240Hrs.	
4	Low Temperature Operating Test		-40℃ ± 2℃ / 120Hrs.	
5	High Temperature and High Humidity Operation Test		60℃, 90%RH 120Hrs.	
6	Thermal Shock Test (Non-operating)		-40±2℃ ~ 25±2℃ ~ 85±2℃ (30Min.) (3Min.) (30Min.) 100Cycles	
7	Vibration Test (Packing)	Frequency: 10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
8	Drop (Packing)	Height: 1 m, each time for 6 sides, 3 edges, 1 angle		

Note 1: For each reliability test, the sample quantity is 3, and only for one test item.

Note 2: The HTHHS test is requested the Pure Water (Resistance > 10MΩ).

■ OUTGOING QUALITY CONTROL SEPCIFICATION

1. Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5℃
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

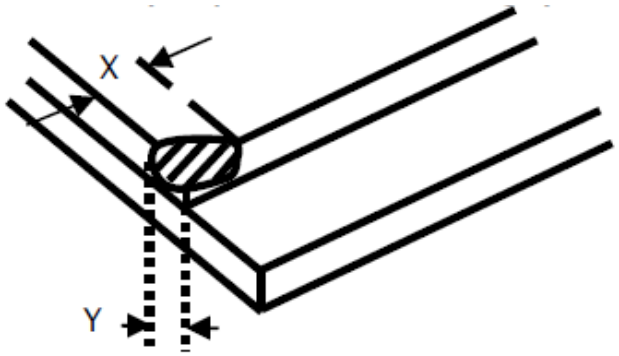
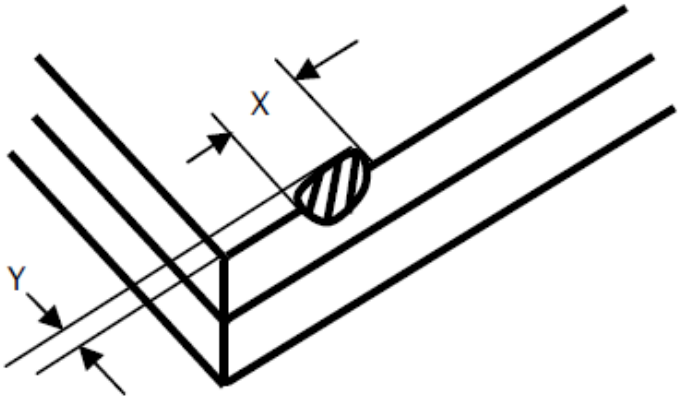
2. Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E.

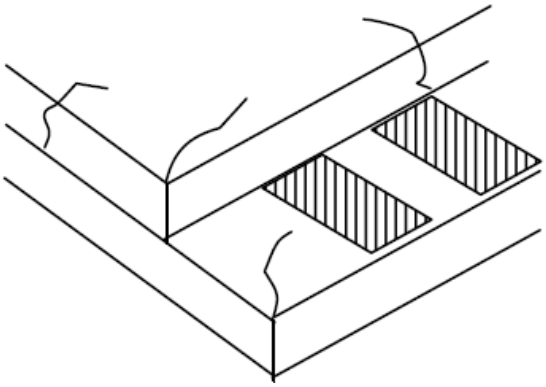
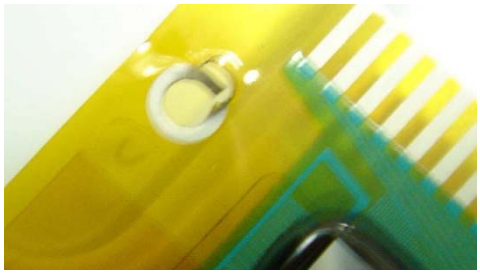
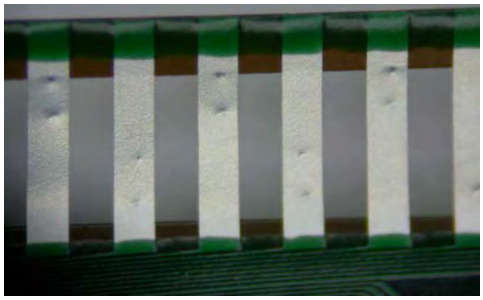
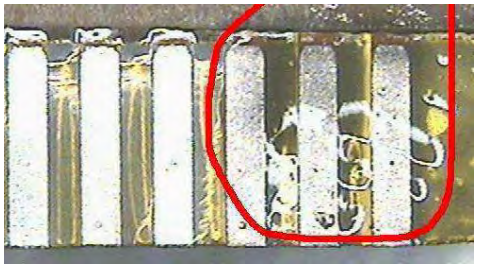
3. Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

3.1 Cosmetic Check (Display Off) in Non-Active Area

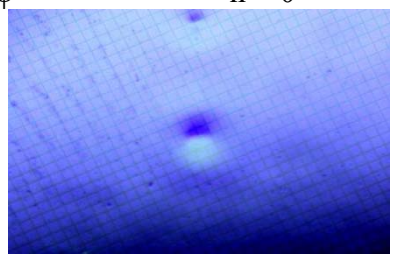
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6mm (Along with Edge) Y > 1mm (Perpendicular to edge)  

3.2 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even pin or Film)	Minor	Not Allowable by Naked Eye Inspection.
Film or Trace Damage	Minor	
Probe Mark on Terminal Lead	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

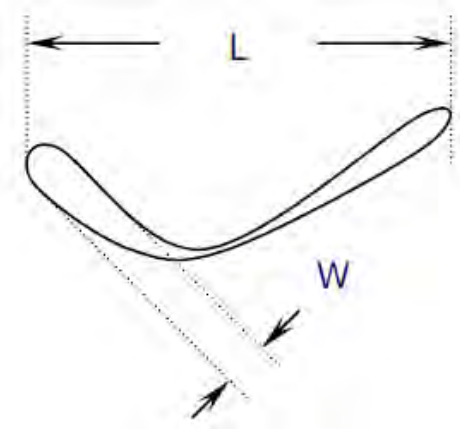
3.3 Cosmetic Check (Display Off) in Active Area

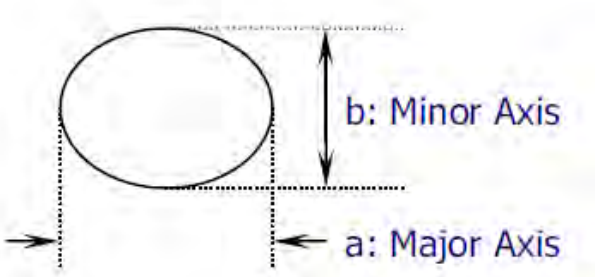
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for not Affect the Panel
Scratches, Fiber, Line-Shape Defect (On Display)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material (On Display)	Minor	φ ≤ 0.1 Ignore 0.1 < φ ≤ 0.25 n ≤ 1 0.25 < φ n =0
Dent, Bubbles, White spot (Any Transparent Spot on Display)	Minor	φ ≤ 0.5 Ignore if no influence on Display 0.5 < φ n = 0 
Fingerprint, Flow Mark (On Panel)	Minor	Not Allowable

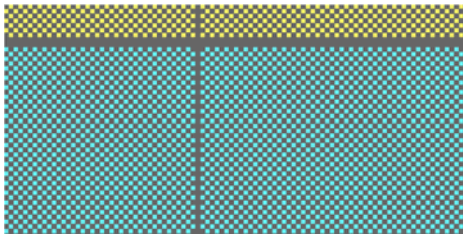
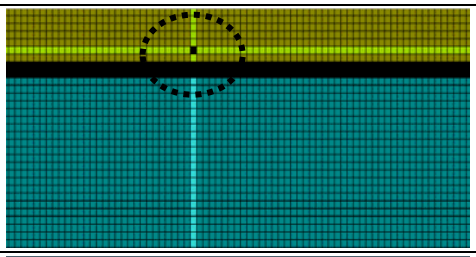
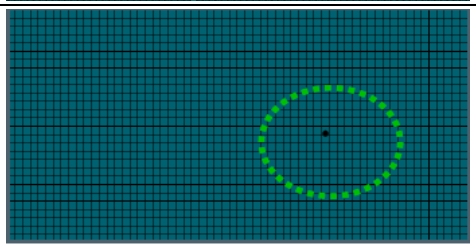
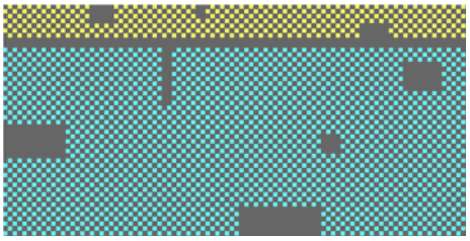
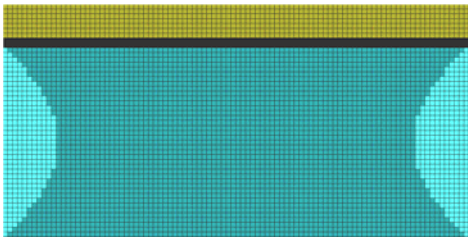
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & φ (Unit: mm): φ = (a + b) / 2





3.4 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

■ CAUTIONS IN USING OLED MODULE

◆ Precautions for Handing OLED Module

1. OLED module consists of glass and polarizer. Pay attention to the following items when handing:
 1.1 Avoid drop from high, avoid excessive impact and pressure.
 1.2 Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 1.3 If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 1.4 Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 1.5 Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 1.6 Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of 1.3.

2. Do not attempt to disassemble or process the OLED Module.

3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.

4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.

5. Be sure to keep the air pressure under 120kPa, otherwise the glass cover is to be cracked.

6. Be careful to prevent damage by static electricity:
 6.1 Be sure to ground the body when handling the OLED Modules.
 6.2 All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 6.3 Do not assemble and do other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%~60% is recommended.
 6.4 Peel off the protective film slowly to avoid the amount of static electricity generated.
 6.5 Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 6.6 Be sure to use anti-static package.

7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.

8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.

9. When the logic circuit power is off, do not apply the input signals.

10. Power on sequence: VDD (logic voltage) ⟶ VCC (driving voltage), and power off sequence: VCC (driving voltage) ⟶ VDD (logic voltage).

11. Be sure to keep temperature, humidity and voltage within the ranges of the spec., otherwise shorten Module's life time, even make it damaged.

12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆ **Precautions for Soldering OLED Module**

1. Soldering temperature: 260℃ ± 10℃.
2. Soldering time: 3~4 sec.
3. Repeating time: no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ **Precautions for Storing OLED Module**

1. If the module cannot be used up in 3 months, make sure to seal the module in the vacuum bag with desiccant.
2. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
3. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
4. It is recommended to keep the temperature between 0℃ and 30℃, the relative humidity not over 60%.

◆ **Limited Warranty**

Unless agreed between All Shore and customer, All Shore will replace or repair any of its OLED modules which are found to be functionally defective when inspected in accordance with All Shore OLED acceptance standards (copies available upon request) for a period of one year from date of production. Cosmetic / Visual defects must be returned to All Shore within 90days of shipment. Confirmation of such data shall be based on data code on product. The warranty liability of All Shore limited to repair and / or replacement on the terms set forth above. All Shore will not be responsible for any subsequent or consequential events.

◆ **Return OLED Module Under Warranty**

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- Broken OLED glass.
- PCB eyelet is damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely.

■ PRIOR CONSULT MATTER

1. For All Shore standard products, we keep the right to change material, process... for the product property without notice on our customer.
2. For OEM products, if any change needed which may affect the product property, we will consult with our customer in advance.
3. If you have special requirement about reliability condition, please let us know before you start the test on our sample.